

Docket No.: 57454-970

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
	:	
Hideto HIDAKA	:	Confirmation Number: 3060
	:	
Serial No.: Divisional of Appln.	:	
Serial No. 09/813,796	:	Group Art Unit: Not yet assigned
	:	
Filed: August 21, 2003	:	Examiner: Not yet assigned
	:	
For:		MIS SEMICONDUCTOR DEVICE HAVING IMPROVED GATE INSULATING FILM RELIABILITY

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

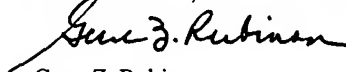
In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The references were cited by or submitted to the U.S. Patent and Trademark Office in parent application Serial No. 09/813,796, filed March 22, 2001, which is relied upon for an earlier filing date under 35 USC 120. Thus, copies of these references are not attached. 37 CFR 1.98(d).

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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SERIAL NO.
**Divisional of Appln. Serial
No. 09/813,796**

FILING DATE
August 21, 2003

GROUP
Not yet assigned

(PTO-1449)

U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		"A Precise On-Chip Voltage Generator for a Gigascale DRAM with a Negative Word-Line Scheme", by Tanaka et al., IEEE Journal of Solid-State Circuits, Vol. 34, No. 8, 8/1999, pp. 1084-1090.
		"Ultra LSI Memory" by Kiyoo Ito, Advanced Electronics Series, November 5, 1994, published by Baifukan, pp. 351-371.
		"An Experimental 256-Mb DRAM with Boosted Sense-Ground Scheme", by Asakura et al., IEEE Journal of Solid-State Circuits, Vol. 29, No. 11, 11/1994, pp. 1303-1309.

DATE CONSIDERED

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.